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B.E. 7th Semester (CSE) Examination,

May-2012

ADVANCED COMPUTER ARCHIECTURE

Paper-CSE-401-E

Time allowed : 3 hours] [Maximum marks : 100

Note : Attempt any five questions .

1. (a) What do you mean by instruction set ? Explain various types of the instruction set. 12
- (b) Differentiate between hardware approach and software approach of designing the control unit. 8
2. (a) Assume a wafer has diameter of 21 cm and cost \$ 5,000 for a particular production run. Compute the cost per die for die area = 2.3 cm^2 for 1 cm^2 if $\rho_D = 1 \text{ defect/cm}^2$. 10
- (b) Explain processor evaluation matrix with suitable example. 10

3. (a) Suppose we have the following parameters for an L1 cache with 4KB and an L2 cache with 64 KB.

The cache miss rate is

4KB 0.10 misses per refr

64 KB 0.20 misses per refr

1 REFR/I

3-CYCLES L1 miss, L2 hit

10 CYCLES total time L1 miss, L2 miss

What is the excess CPI due to cache misses?

10

- (b) What is the principle of locality? Explain various types of locality. 10

4. (a) Explain the Strecker's Memory model in detail. 10

- (b) Explain the open, closed, and mixed queue models in detail. 10

5. Explain different types of shared memory multiprocessors. Also discuss memory coherence in shared memory multiprocessors. 20

6. What is the use of micro program sequencer in micro programmed control unit ? Also describe the working of micro program sequencer. 20

7. Assume we have a vector processor with the following parameters :

Processor cycles = 10 ns

S, the number of simultaneously memory request per cycle = 2

$T_c = 60$ ns

T, cycles per $T_c = 6$

M, modules = 16.

Compute the worst case performance and relative performance.

8. Write short notes on the following :

- (a) Split cache
- (b) Queuing theory
- (c) Page replacement
- (d) Hellermans model.